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Research Article

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Structure-Property Correlation in Ir Transparent Zinc Sulphide (Zns) Ceramics Under Chemical Vapour Deposited & Hot Iso-Statically Pressed Conditions

M Buchi Suresh* and Roy Johnson

Centre for Ceramic Processing, International Advanced Research Centre for Powder Metallurgy and New Materials (ARCI), Balapur, Hyderabad, Telangana, India

***Corresponding author**
M Buchi Suresh, Centre for Ceramic Processing, International Advanced Research Centre for Powder Metallurgy and New Materials (ARCI), Balapur, Hyderabad, Telangana, India-500005; E-Mail: suresh@arci.res.in

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Abstract

IR Transparent ZnS ceramics processed through chemical vapour deposition were subjected to Hot Isostatic pressing and the samples in both the conditions were characterized by XRD, microstructure and high temperature impedance spectroscopic studies for the dielectric and electrical properties. Both the samples have shown cubic sphalerite phase with enhanced orientation along (111) plane as a result of hot isostatic pressing as revealed by XRD.HIP treatment to ZnS facilitated the enhancement of the homogeneity of microstructure and enhancement in the grain size from 10μm to 50μm. The electrical behavior of both the samples was investigated by AC impedance spectroscopy in the frequency range 1Hz to 1MHz from RT to 500°C in dry air. HIP has resulted in a significant increase in the dielectric constant, which can be attributed to the increase in homogeneity and the grain size. Further, the complex impedance plots exhibited two impedance semicircles identified in the frequency range is explained by the grain and grain boundary effects. An equivalent-circuit analysis of AC impedance spectra based on the brick-layer model was performed. Activation energies obtained from the conductivity plots indicates an Arrhenius type thermally activated process.

Keywords: CVD, Complex Impedance, Grain Boundary Conduction, Activation Energy, Transparent Zns Ceramic

Introduction

IR transparent ceramics become more and more important for thermal imaging applications in which materials are expected to achieve almost theoretical transmission in combination with desired mechanical, electrical and thermal properties to withstand harsh environments [1,2]. In view of this, the development of new optoelectronic devices has extended the use of ordinary optical materials to new applications and environments such as temperature (IR) sensor, optical fiber communications, laser interferometers, etc [3]. Most of the transparent ceramics are single crystals that are grown from the melt or by fusion at relatively high temperatures. However, the crystal growth is time consuming followed by machining which is an expensive task that limits the scale up of production and hence limiting their wide range of applications. For this reason, the current trend moves towards the production of polycrystalline transparent ceramics from starting powders, which permit the easiness of substituting single crystal by providing more versatile properties and to produce complex shapes, that widens the field of application. Compared to single crystals, polycrystalline materials have a complex microstructure consisting of grains, grain boundaries, secondary phases and probably residual pores. However, the major challenge is achieving the transmission to the close theoretical density >99.9% and retaining the grain size as less as possible to attain superior optical and mechanical properties. Although, previous researchers have studied optical and structural properties of IR transparent polycrystalline ZnS and other ceramics, only few studies are reported room temperature electrical properties, and no report is found on high temperature (500oC) impedance spectroscopic studies [4-13].

In our previous studies, bulk ZnS ceramics were processed by chemical vapour deposition and its mechanical and optical properties were reported [14]. In this work, high temperature dielectric and electrical characterization of ZnS ceramics in CVD and post CVD HIPed condition were studied and the results are correlated with the processing parameters such as crystallite size, microstructure, etc.

Experimental Procedure

ZnS ceramics were processed using chemical vapour deposition technique using the precursors such as Zn metal and H2S gas. The details are presented in our previous work [14]. The CVD processed ZnS samples were Hot Isostatically Pressed at 975°C for 5h under 1500 bar pressure in Argon environment. The processed samples were characterized by X-ray diffraction technique using (D8 Advance, Bruker, Karlsruhe, Germany) diffractometer irradiated with CuKα radiation of wavelength λ=1.54A° in the diffraction angle range 20-80°. The microstructure of the samples was recorded using scanning electron microscopy (S-4300SE/N, Hitachi, Tokyo, Japan). ZnS ceramic samples without and with HIP treatment were polished,

ultrasonic cleaned with acetone and dried at 100 °C. Silver paste was then deposited and the organic solvent was removed. Solartron make SI1260A impedance analyzer is used to measure the dielectric and electrical properties of CVD processed ZnS sample and HIPed ZnS sample. Impedance measurements were taken on a two electrode configuration cell, in dry air, from RT to 500 °C in 50 °C steps.

Results and Discussion

X-ray diffraction (XRD) patterns of CVD processed and post CVD HIPed ZnS samples are shown in Figure 1(a-b). All the peaks are indexed according to the standard XRD pattern of the ZnS (ICDD PDF 80-0020). With the HIP treatment, there is an increase in intensity and narrowing of the diffraction peaks, indicative of better re-crystallization and resulting grain growth. Crystallite size is found to increase from 21nm to 68nm. It is obvious from the peaks of HIPed sample that as the sample is hot isostatically pressed, there is a decrease in the full width at half maximum (FWHM) due to improved densification and grain morphology by simultaneous application of pressure and temperature and hence the crystalline size increases due to grain growth during HIP treatment including both the heating up process and dwelling process.

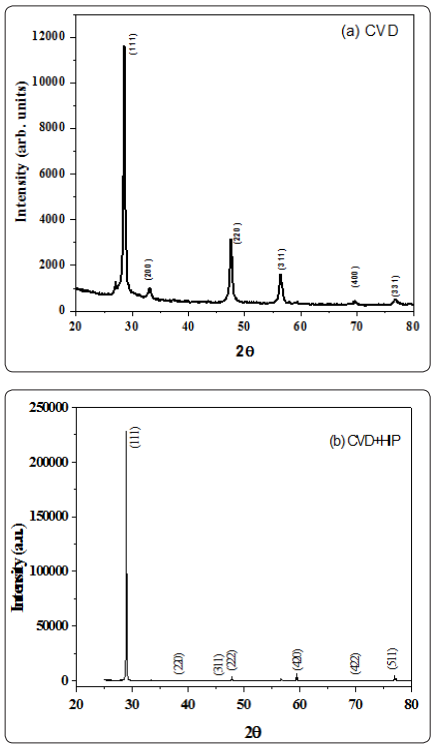

Figure 1: (a-b) XRD patterns of ZnS ceramics (a) CVD (b) CVD+HIP

Figure 2(a-b) shows the scanning electron microscopy images of CVD processed ZnS sample and post CVD ZnS sample with HIP treatment. As can be seen, the CVD processed ZnS sample is composed of columnar structured grains with residual porosity, characteristic of CVD. Hot Isostatic Pressing of CVD ZnS ceramic resulted into complete dense microstructure with faceted grains. Average grain size of CVD processed ZnS and HIPed ZnS samples were estimated by linear intercept method of the SEM images and were in the range of 10 and 50 µm, respectively for CVD and post CVD HIPed samples. A substantial increase in grain size by a factor of 5 is observed as a result of HIPing, as the temperature of HIPing is carried out at the elevated temperature of 950°C in comparison to the CVD ZnS sample.

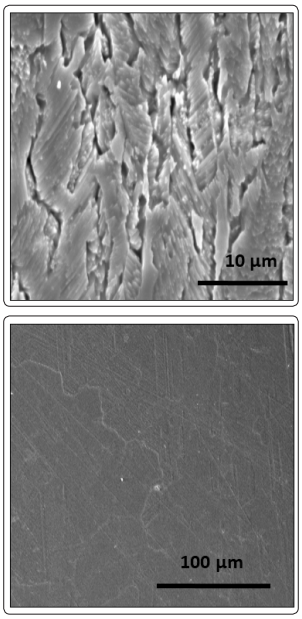

Figure 2: (a-b) SEM images of ZnS ceramics (a) CVD (b) CVD+HIP

Frequency dependency of dielectric properties of ZnS ceramics under two different conditions are shown in Figure 3. The dielectric constant of CVD ZnS sample with smaller grain size is more than that of the HIPed sample with larger grain size. It is well known that the dielectric constant of the grain is lower than that of the grain boundary so that the dielectric constant of ZnS sample with smaller grain size is higher in the low frequency region. Whereas, in the high frequency region, dielectric constant is almost independent of frequency and is observed to be same in both the samples. In the lower frequency regime, dipoles in atomic structure are still able to follow the external field oscillation, whereas, in the high frequency region, these dipoles begin to fall behind the external field and the value of dielectric constant tends to change slightly, which indicates the saturation state of polarization [15-17].

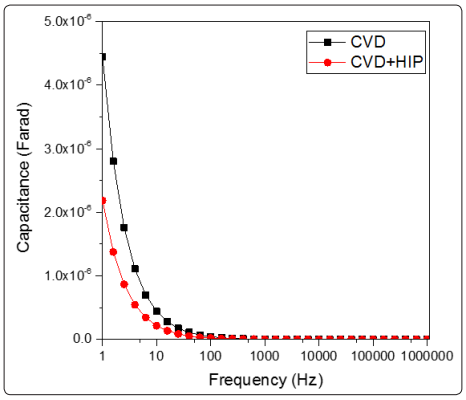

Figure 3: Capacitance versus frequency of ZnS CVD and ZnS CVD+HIP

Figure 4(a-c) shows the variation of real part of impedance with

frequency at different temperatures of ZnS ceramics. It is known that Z' is related to the sample electrical resistance and Z' value decreases with the rise of the frequency and temperature. The decreasing nature in the magnitude of Z' with increasing temperature in the present study suggests the typical negative temperature coefficient of resistance type behavior of the material. The variation of Z' shows a plateau up to certain frequency followed by a steep dispersion and then almost merges for all the temperatures implying the absence of space charge polarization at high frequency in the ZnS ceramic. The observed low frequency plateau is mainly attributed to the grain boundary response of the material. Significant increase in the low frequency plateau region with HIP treatment indicates that the grain boundary resistance is enhanced by HIP treatment. In the high frequency regime, the impedance is almost constant in the complete range of measured temperature and frequency indicating a possible release of space charges those have induced a reduction in barrier property of the material with increasing temperature which may be a responsible factor for the enhancement in ac conductivity of the material with temperature at higher frequencies.

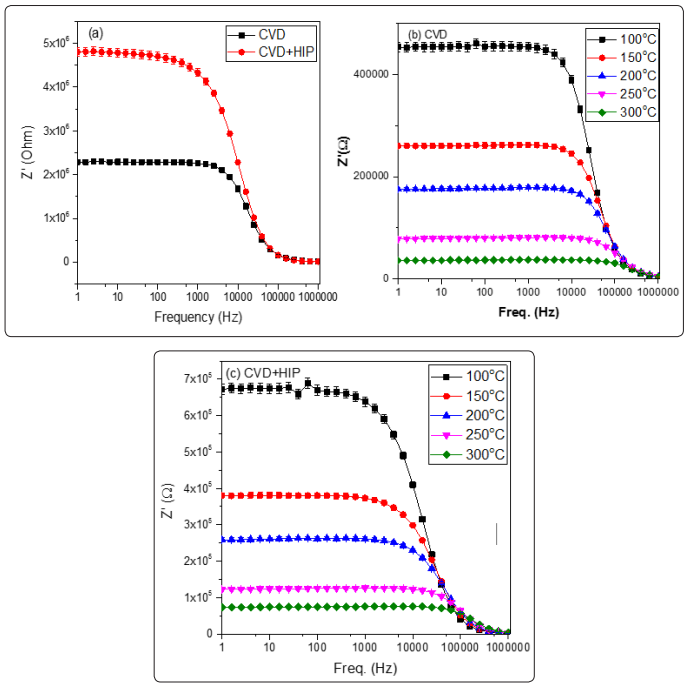

Figure 4: (a-c) Real part of impedance versus frequency of ZnS ceramics

Figure 5 shows the variation of imaginary part of impedance with frequency at different temperatures for CVD processed and post CVD HIPed ZnS samples. These plots show a single peak at all the temperatures and as the temperature increases, the value of the peak decreases resulting in increase in the conductivity. It is found that initially the magnitude of imaginary part of impedance increased slowly in the lower frequencies and then increases significantly up to a frequency called resonant frequency and then decreases beyond resonant frequency. At the peak maximum, the value of impedance increased by HIP treatment of ZnS ceramic. Similar behavior is observed at all the temperatures. The peaks shift with increase in temperature towards higher frequencies, and the curves tend to come closer and merge at higher frequencies. The height of the peak is proportional to the resistance of phases present in the system, while the position of the relaxation frequency indicates the ability of charge carriers to follow AC signals. The increase in relaxation frequency with temperature indicates an increase in the rate of hopping of localized charge carriers. The peaks shift towards higher frequencies with the increase in temperature, and the dispersion curves tend to merge at higher frequency, indicates thermally activated dielectric relaxation process and a possible release of space charges in the material.

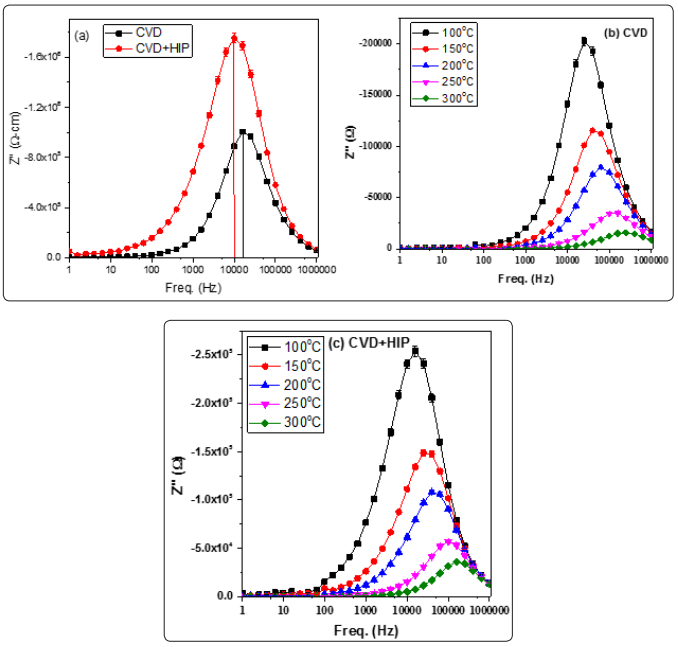

Figure 5: Imaginary part of impedance variation with frequency at different temperatures for ZnS ceramics with and without HIP treatment

To evaluate the nature of relaxation behavior concerning the charge transport mechanism such as electrical transport and conductivity relaxation and to distinguish long range conduction from short range hopping motion, frequency dependence of imaginary part of electric modulus is studied for both the samples. The combined plots of Z" and M" versus frequency for CVD processed and post CVD HIPed ZnS ceramic samples are shown in figure 6(a-b). These plots give information about the dominant relaxation process of charge carriers by short range or long range movement. The low frequency side of the peak represents the region in which charge carriers are mobile at long distances, ie., charge carriers can migrate successfully via hopping from one site to its neighboring site. Above the peak frequency the charge carriers are localized within the potential well and have short range localized motion. The separation of peak frequencies between Z" and M" indicates that the relaxation process is dominated by the short range transport of charge carriers and deviates from an ideal Debye behavior and the presence of a relaxation time distribution.

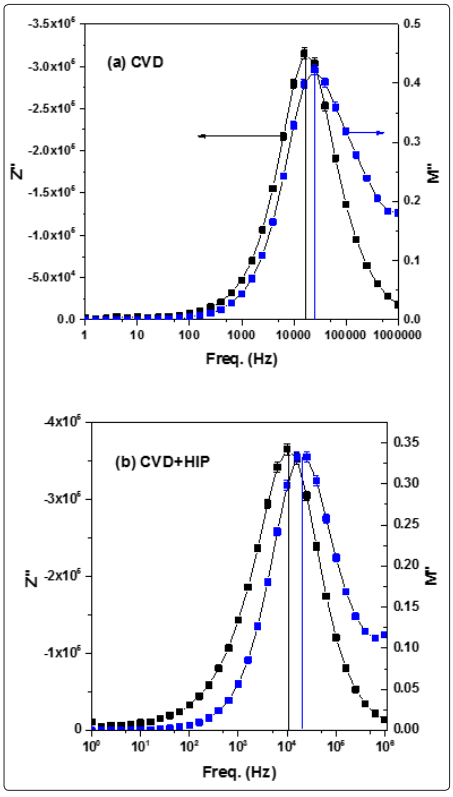

Figure 6: (a-b) Z" and M" versus frequency plots of CVD and CVD+HIP samples

Typical Cole-Cole plots of CVD processed and post CVD HIPed ZnS ceramics are shown in figure 7(a-c). The impedance spectra of the CVD sample with average grain size of 10 µm exhibited single semicircular arcs in the measured frequency range, whereas the spectra of the sample with large grain size of 50 µm was apparently single but depressed half circle in the low frequency regime. The observation of depressed semicircles suggested that the brick-layer model could be employed for further analysis. As per the model, depressed semicircle is due to combination of two semicircles with their centers on the positive axis in the polycrystalline ceramic material. Accordingly, the semicircle at high and low frequencies may be assigned to charge transport within the crystallites and a grain boundary effect, respectively. Separate semicircular arcs were attributed to different conduction mechanism based on their time constants. In general, the grain boundary effect on electrical conductivity may originate from a grain boundary potential barrier or from space charge layers which are depleted in majority charge carriers and are localized along the grain boundaries. The total resistance is measured from the intercept of the semicircles at low frequency side and conductivity is calculated using $\sigma=t/(R*A)$, where t-thickness, A-electrode area, R-resistance. The conductivity is found to increase with increase of temperature in both the samples. This increase is due to increase in the rate of thermally activated electron hopping and release of trapped charge carriers with increasing temperature. Hence, it is clear that the measured impedance spectrum is typical for polycrystalline ionic conductors in which the ionic current is partially blocked by the grain boundaries.

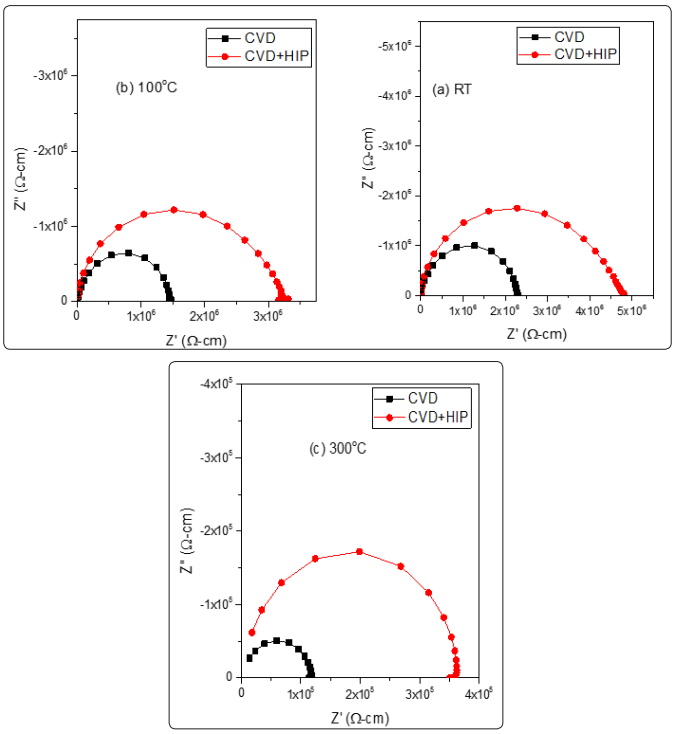

Figure 7: (a-c) Cole-Cole plots of ZnS samples of CVD and CVD+HIP at different temperatures

In order to see the effect of grain size, grain boundary resistance is calculated and plotted against temperature for both the samples (Fig. 8). It is clear from the figure that grain boundary resistance is higher in post CVD HIPed sample compared to the CVD processed ZnS sample due to increase in the grain size. Moreover, the blocking factor calculated is found to be higher in post CVD HIPed sample ($\alpha_{300°C}$=0.26 for post CVD HIPed sample and $\alpha_{300\,°C}$=0.19 for CVD processed ZnS sample) indicating that the conduction path through grain boundary is less.

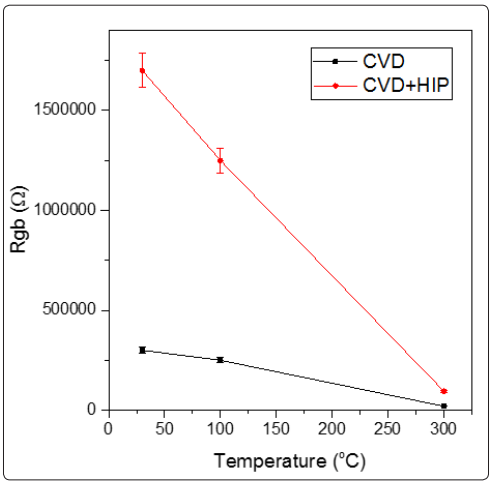

Figure 8: Variation of grain boundary resistance with temperature

The behavior of Cole-Cole plot result in one semicircle with a large values of depression angles. This can be related to heterogeneity in the sample. Therefore, a better fitting was made with two semicircles. A least-square fit of the equivalent circuit along with the impedance plot is shown in Fig. 9(a-b), and the resulting values for the fit-parameters are given. In the present case, semicircles are depressed to some extend and more in lower frequency regime, so these were fitted with parallel resistances and constant phase elements instead of RC elements to accommodate the non-Debye type behavior due to the presence of more than one relaxation process occurring within the system with comparable relaxation times.

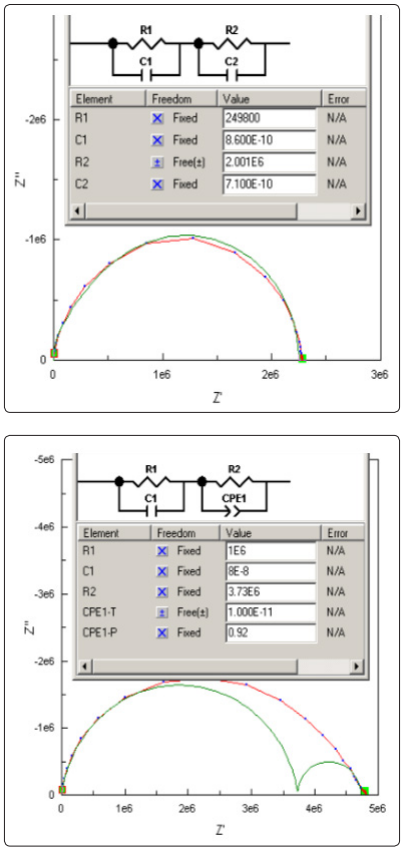

Figure 9: (a-b) Fitted Cole-Cole plots with equivalent circuits of CVD and CVD+HIP ZnS ceramics

Figure 10 shows the Arrhenius plots of CVD processed ZnS and post CVD HIPed ZnS samples. A significant decrease in the conductivity due to increase in grain size is evident from the figure. The plots are fitted to straight lines and activation energies are evaluated from the slopes of the fitted lines. Activation energies for conductivity were calculated using $\sigma=(\sigma_o/T)\exp(-Ea/\mathbf{k}T)$, where σ is the conductivity, so is a pre-exponential constant, **Ea** is the activation energy for conductivity, **k** is Boltzmann's constant and **T** is temperature. CVD sample has given an activation energy of 0.42eV and decreased to 0.38eV with HIP treatment. The calculated activation energy values are in good agreement with the reported values [15]. It can be observed that Ea decreased with HIP treatment which can be attributed to an increase the charge carrier mobility and decrease in defect levels. The conduction process can be explained by the grain boundary barrier effect. It is known that a polycrystalline material contains a large number of grains separated by grain boundaries and the grain boundary consists of a couple of atomic layers of disordered atoms that produce large number of defects, these defects impede the transit of carriers from one grain to the other acting as potential barriers. The height of the barrier is a function of the grain size, hence grain size and grain boundary density in polycrystalline ceramic influence the electrical conductivity. The presence of grain boundaries results into inter-grain depletion layers and to Schottky energy barriers, change in the depletion layer width and energy barrier height at each grain that causes a change in the resistance of the material [18].

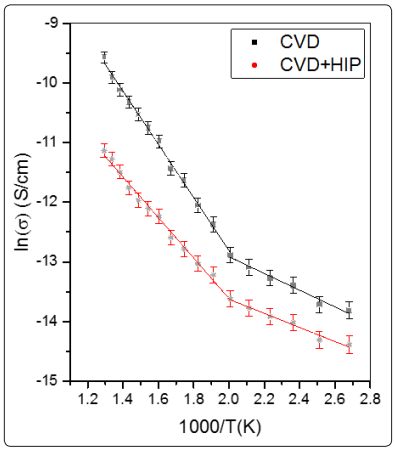

Figure 10: Arrhenius plot of conductivity of ZnS Ceramics of CVD and CVD+HIP

Frequency dependence of the electrical conductivity for CVD processed ZnS ceramics prepared from CVD process and Hot Isostatically Pressed is shown in Figure 11. It is revealed that with the frequency growth, the conductivity value increases. Two dispersion regions caused by the ion transport in the grain boundaries and in the bulk of ZnS ceramics are observed in the frequency range under investigation. Such type of frequency dependencies of electrical conductivity indicates relaxation processes: the high frequency parts of the spectra can be attributed to the relaxation in the bulk, while the lower parts correspond to grain boundary processes.

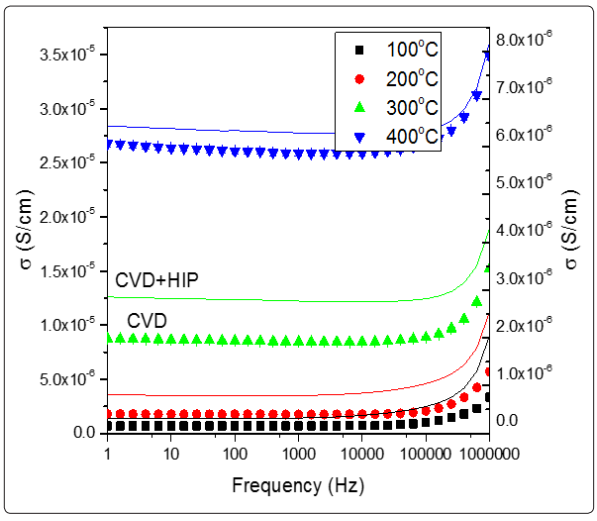

Figure 11: Conductivity variation with frequency at different temperatures of ZnS ceramics of CVD and CVD+HIP

Therefore, the major difference in electrical conductivity between the samples with different grain size can be explained by the significant grain boundary resistance effect in ZnS. The second factor owing to grain size, which can alter the electrical conductivity of a polycrystalline oxide, is the GB effect. In principle, the bulk conductivity of a grain does not change with respect to grain size. However, the apparent conductivity of a polycrystalline material varies with the grain size because the GB volume fraction is changed. In contrast, the resistance of GB is inversely proportional to the grain size, because the number of grain boundaries per unit length, which are connected in series, increases with decreasing grain size [19-22]. Therefore, the portion of grain boundary resistance contributing to the total resistance of the sample increases with decreasing grain size. The temperature dependence of electrical conductivity showed a clear variation, which signifies that, the effect of grain size plays an important role in the electrical transport properties of ZnS ceramics. Our results are in good agreement with the reported data.

Conclusions

ZnS Ceramics are prepared by chemical vapor deposition technique and Hot Isostatically Pressing is carried out on CVD samples to achieve close to theoretical density. No structural changes are observed by HIPing the ZnS ceramics except highly preferred orientation in (111) plane. HIPing has resulted in the homogeneous faceted microstructure in comparison to columnar microstructure observed with CVD processed samples. A substantial increase in the grain size by a factor of 5 is observed as a result of HIP carried out at the elevated temperature of 950 °C in comparison to the CVD ZnS sample. Complex impedance spectroscopy reveals grain and grain boundary contributions to the total conductivity of the specimens. The relaxation process occurred in the ZnS ceramic is non-Debye type in nature and is explained by considering constant phase element. The equivalent circuit model has changed from R-C to R-CPE. Further activation energies obtained confirmed the presence of vacancies. Decrease in vacancies has been found to be responsible for the increase in impedance.

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