Short Article

Open Access Journal of Applied Science and Technology

Nano Electro Magnetic Full Adder

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Submitted: 2023, Jun 01; **Accepted:** 2023, Jun 26; **Published:** 2023, July 14

Citation: Khalesi, E. (2023). Nano Electro Magnetic Full Adder. *OA J Applied Sci Technol, 1*(2), 56-59.

Abstract

In this paper, I proposed new idea for a nano, electromagnetics Full adder. Simulation and design of inverter and majority voter is a work on Bonhemmi method and analysis that is based on SST.MTJ method. After this idea, we can design other gated and devices besed on this formula to implement Microprocessor and ... Spintronics devices are based on the up or down spin of the electrons rather than on electrons or holes as in the traditional semiconductor electronics devices. Magnetic processors using spintronics devices in principle are much faster and with the potential features of nonvolatile, lower power consumption and higher integration density compared with transistor-based microprocessor. Full adder is one of the most important basic units of the arithmetic/logic unit for any processors. The design of the full adder determines the speed and chip-density of a processor. In this paper, a novel spintronics full adder is proposed based on novel programmable spintronics logic devices. Only seven magnetic tunnel junction elements are needed for this full adder design.

Keywords: Full Adder, MTJ, SST Full Adder, Bonhemmi Method

1. Introduction

The Introduction section, of referenced text expands on the background of the work (some overlap with the Abstract is acceptable). The introduction should not include subheadings.

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2. Spintronics

In Bonhomme Model, a Circuit Modeling of Spintronic Devices by SPICE Implementation has observed. The model of Inverter in this Design is based on this theory.

Magnetic domains were postulated as a way to explain the hysteretic characteristics of a magnetized material. Weiss postulated that a "molecular" field is present that balances the thermal motion of particulars. This field is justified by the quantum mechanical exchange forces present in ferromagnetic materials and it explains the magnetization curves of ferromagnetic materials.

Spintronic devices utilize ferromagnet elements that are composed of only a single domain. Single domain ferromagnets exist when the dimensions of the sample are sufficiently small such that domain formation is impossible due to the fact the total energy of the sample is minimized as a single domain permanent magnet. In general, these dimensions occur when the Barkhausen effect becomes negligible. In Fe, Ni, and Co this occurs around 10−7m.

The 2-channel resistor model, 2, predicts the steady-state behavior of ferromagnetic devices with collinear magnetizations, m~ 1, ±m~ 2. This leads to phenomena such the Giant 11 Magnetoresistance (GMR) which is already well understood in other devices with ferromagnetic elements, such as the Magnetic Tunnel Junction (MTJ). The model splits the spin dependent quantities into spin up, ↑, and spin down, ↓ polarizations, essentially identical to the majority and minority carrier concentrations present in semiconductor transport. Separate branch currents are used in the circuit for spin up current, I↑, and spin down current, I↓. This results in separate conductance's, G↑ and G↓ that represent the conductance of majority and minority spins as shown in Fig. 2

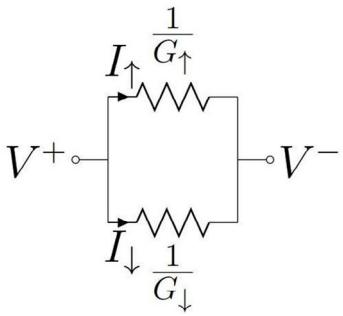

Figure 1: Two-Channel Resistor Model.

The development of an equivalent circuit for the magnetization dynamics requires refactoring the LLG equation, which is restated here:

$$\frac{d\vec{m}}{dt} = -\gamma_0\mu_0\left(\vec{m}\times\vec{H}\right) + \alpha\left(\vec{m}\times\frac{d\vec{m}}{dt}\right) + \frac{\vec{m}\times\left(\vec{I}_s\times\vec{m}\right)}{qN_s},$$

where we have divided by the saturation magnetization, Ms, in order to normalize the dependent variable, m~ , and the effective magnetic field, H~ = Hk ~h. Equation 39 can be written as a system of differential equations in terms of dm~ dt by taking the cross products and 21 writing the resulting system,

$$\begin{aligned}
\frac{dm_x}{dt} &= \left(\frac{dm_z}{dt}m_y - \frac{dm_y}{dt}m_z\right)\alpha - \left(H_{\text{eff},z}m_y - H_{\text{eff},y}m_z\right)\gamma\mu \\
&\quad + \frac{-I_{S,y}m_xm_y + I_{S,x}m_y^2 - I_{S,z}m_xm_z + I_{S,x}m_z^2}{N_sq}, \\
\frac{dm_y}{dt} &= \left(-\frac{dm_z}{dt}m_x + \frac{dm_x}{dt}m_z\right)\alpha - \left(-H_{\text{eff},z}m_x + H_{\text{eff},x}m_z\right)\gamma\mu \\
&\quad + \frac{I_{S,y}m_x^2 - I_{S,x}m_xm_y - I_{S,z}m_ym_z + I_{S,y}m_z^2}{N_sq}, \\
\frac{dm_z}{dt} &= \left(\frac{dm_y}{dt}m_x - \frac{dm_x}{dt}m_y\right)\alpha - \left(H_{\text{eff},y}m_x - H_{\text{eff},x}m_y\right)\gamma\mu \\
&\quad + \frac{I_{S,z}m_x^2 + I_{S,z}m_y^2 - I_{S,x}m_xm_z - I_{S,y}m_ym_z}{N_sq}.
\end{aligned}$$

3. Method

A simplified circuit model of an ASL device is shown in Fig. 14 which indicates the majority logic functionality that ASL devices are capable of performing. In this illustration, the capacitors represent the magnetizations of the ferromagnets present in ASL devices. The inverter represents the polarity of the logical operation performed, since for positive bias voltages ASL is complementary in nature. Each ferromagnet serves as an input logic bit, with an additional ferromagnet used to bias the structure. We can think of this device as an N-input NAND/NOR logic gate, where the polarity of the magnet mb determines whether the device behaves as either a NAND gate or a NOR gate.

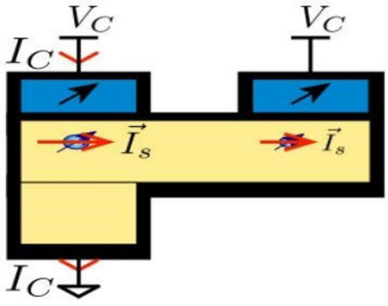

Figure 2: All Spin logic Inverter Illustration

The ASL inverter is biased by applying a voltage at the ferromagnet terminals. Qualitatively, the device functions by shunting all DC charge current from the input magnet into 34 Figure 15: All-Spin Logic Inverter Illustration. the ground channel. This is possible since the resistance between the input and output ferromagnets is small, thus minimizing the amount of charge current in the channel. Equation 29 predicts that in the collinear case, the spin current along the ±x direction at the FM/NM interface is, Is,x = Vs,xG↑ + VCG↓.

Also, All-Spin Logic functions by storing the state of a boolean variable in the magnetization of an output ferromagnet. A non-magnetic conductor then connects the output ferromagnet to an input ferromagnet. The applied bias voltage determines the function of the device, where positive bias voltages cause the output ferromagnet to invert, while negative bias voltages cause the output ferromagnet to copy the state of the input ferromagnet. This mode of operation is what drives the first device will study, a boolean logic inverter. We will then extend the ASL inverter into a majority gate capable of the NAND/NOR boolean logic functionality.

Each ferromagnet serves as an input logic bit, with an additional ferromagnet used to bias the structure. We can think of this device as an N-input NAND/NOR logic gate, where the polarity of the magnet mb determines whether the device behaves as either a NAND gate or a NOR gate.

We can utilize the models developed in this work to construct boolean logic devices that are capable of NAND and NOR logic operations, in addition to the invertering logic circuit shown in Fig. 15. This is accomplished by treating each input of the majority logic as an input ferromagnet, and constructing multiple interconnect and ground channels for each input. The channels are then connected to an output ferromagnet as shown in Fig. 18.

We have constructed a device that behaves as a majority gate capable of the boolean NAND and NOR operations. The magnets m~ 1 and m~ 2 serve as inputs while m~ C is used to bias the device as a NAND or NOR gate. When the bias magnet is configured in the −x direction, the device behaves as a NAND gate. When biased in the +x direction the device functions as a NOR gate. The transient simulation of the ASL majority gate is shown in Fig. 19 for both the NAND and NOR functions.

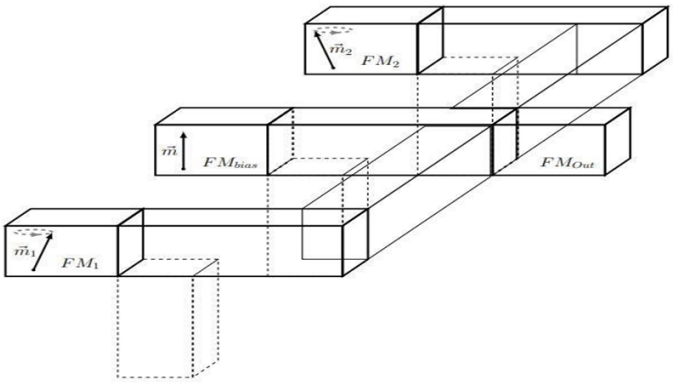

Figure 3: Majority Gate

This MTJ Full adder has implemented in LTSPICE. For circuit modulation, as you see in Fig 7. By having MTJ Inverter and Majority. Voter , the circuit has implemented. For design in SPICE, I have implemented Full adder by having Inverter and Majority. Voter and in figure of BLOCKS in SPICE. My suggestion for wires for implement other gates and microprocessor is usage of nanowires, if it would be possible. For input o circuit, I implemented Pulses that gave me final result.

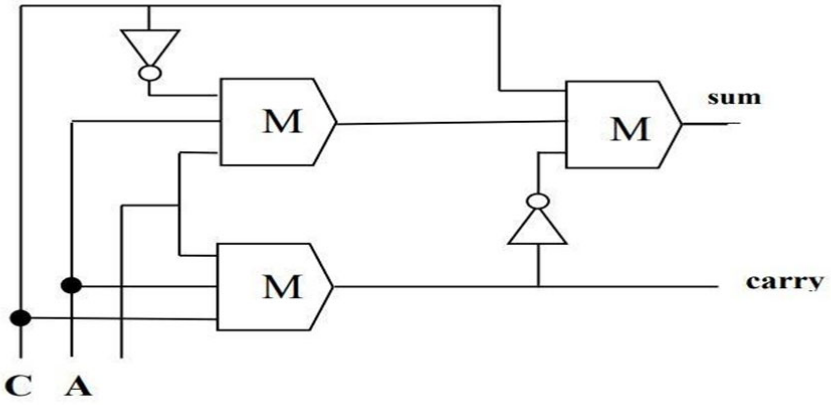

Figure 4: Schematic Design of Full Adder

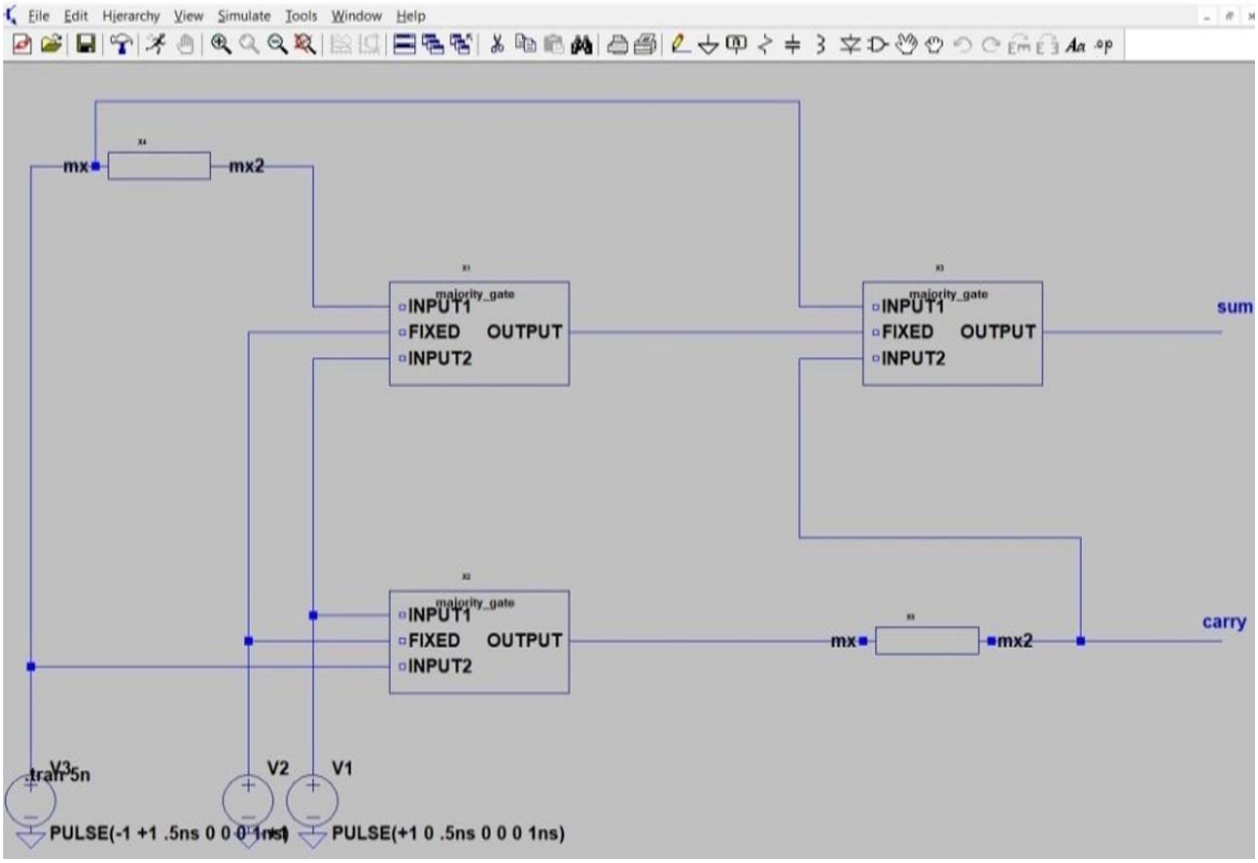

Figure 5: Simulation of Nano Full Adder in SPICE by use Block

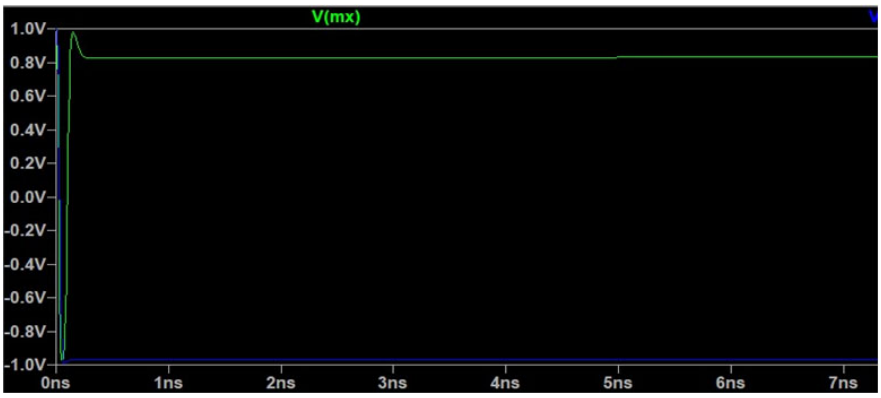

Figure 6: Result in SPICE

4. Conclusion

For final result, firstly implement Majority Gate and Inverter in spice based on Bonhemmie Theory and then by implement the Full Adder, as Figure 4 by having pulse input I got final result. My suggestion for wiring in IC's is implement Nanowires, maybe for production CPU helps to have better results in IC Industry [1-10].

Acknowledgement

I want to declare my thankfulness from POLITO University and Group for efforts in MRAM Project which was my guide to obtain a design for a MTJ Full. Adder.

Competing Interest

The author declare competing Nonfinancial Interests and following Competing Financial Interest.

Author Contribution

Please include "Author Contribution" section in the main article, specially stating what each author contributed to. Since this is a single author paper kindly specify the same in the manuscript.

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