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Research Article

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Growth C-Axis Zno Nanowires By Upturned Crystalline Growth Method on P-Si(111) Substrate

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Abstract

The using method a low temperature and low cost growth method of high quality active materials for optoelectronic devices. ZnO nanowire arrays growth on p-Si(111). The effects of thermal annealing on the optical properties of ZnO nanowires were prepared on sol-gel ZnO-seed-coated substrates. Atomic Force Microscopy (AFM) AFM and... AFM images were found at 130 °C well aligned vertically, and the well defined crystallographic planes, providing a strong evidence that the nanowire arrays orientate along the c-axis. The annealing temperature of the ZnO thin film plays an important role on the microstructure of the ZnO grains and then the growth of the ZnO nanowire arrays.From PL spectra, an evident ultraviolet near-band edge emission peak at 382 nm is observed. From (I-V) characteristic that the material behaves p-n junction diode, ideality factors >> 2.0, that was attributed to tunneling via deep levels in the forbidden gap. Impedancespectra shows the spectrum of the Impedance resistance that the curve does not represent a regular semicircle and this indicates that the structure of the material is not regulated granules but rather is in a different form which is the nanowires .

Keywords: C-axis ZnO nanowires , ZnO seed layer, Sol-Gel , AFM images, Pl spectra, (I-V)characteristics, Ideal factor, Impedance spectra.

Introduction

Zinc oxide is a wide direct band gap (3.37 eV) semiconductor with a large exciton binding energy (60 meV), a hexagonal crystal structure , exhibiting near UV light emission, transparent conductivity, and piezoelectricity, has received much attention due to its potential applications in the optoelectronic field [1-2]. One-dimensional ZnO nanostructures such as nanowires have been extensively studied for other applications including solar cells, ultraviolet (UV) light-emitting diodes, photonic crystals and transparent electrodes [3-6]. Several methods have been demonstrated to fabricate one-dimensional ZnO nanostructures, such as vapor liquid solid epitaxy (VLSE), chemical vapor deposition (CVD) , and pulse laser deposition (PLD) , but these techniques still have some limitations for substrate size and the need for high temperature operation [7-8].

Recently, the growth of ZnO nanowires in phase solutions at low temperature (below 100 °C) was reported by using the hydrothermal process , the growth had been on glass , silicon wafer and plastic substrates [9] . This method shows that the shape of the ZnO nanowires was sensitive to the orientation of Si substrate via the use of ZnO nanoparticles as a seed layer. However, systematic research on the influence of quality characteristics of ZnO sol-gel thin films on the growth of ZnO nanowire arrays via hydrothermal method has rarely been reported. In this work, now catalytic method and ZnO, cost effective, non-catalytic method and ZnO sol-gel thin films were used as the seed layers with different temperatures annealing.

Experimental details

Upturned crystalline growth method is two phases :

Preparation seed layer thin films

The ZnO thin films served as the seed layers were deposited on silicon substrates by a sol-gel method [10]. A coating solution contained zinc acetate dehydrate ($Zn(CH_3COO)\ 22H_2O$, Merck, 99.5% purity) and equivalent molar monoethanolamine (MEA) ($NH_2CH_2CH_2OH$, Merck, 99.5% purity) dissolved in 2-methoxyethanol (2MOE) ($CH_3OCH_2CH_2OH$, Merck, 99.5% purity). The concentration of zinc acetate was chosen to be 0.5 mol/L . The resulting solution was then stirred at 60 °C for 2 h to yield a homogeneous solution, whichserved as the coating solution after being cooled to room temperature. Then the solution was coated onto p-type silicon (111) substrates by a spin coater at the rate of 1000 rpm for 30 s at room temperature. Subsequently, the films were preheated for 10 min to remove the residual solvent. Then the layer film were annealed in a furnace at different temperatures ranging from 130 to 900 °C for 2 h.

Growth Vertical ZnO Nanowires arrays

After uniformly coating the silicon substrates with ZnO thin films,

growth of ZnO nanowire arrays was achieved by suspending these ZnO seed-coated substrates upside down in a glass beaker filled with solution of 50 mM zinc nitrate hexahydrate ($Zn(NO_3)$ $26H_2O$, 98% purity) and 50 mM hexamethylenetetramine (HMT) ($C_6H_{12}N_4$, 99.5% purity). During the growth, the glass beaker was heated with a laboratory oven maintained at 60 °C for 12 h. At the end of the growth period, the substrates were removed from the solution, then immediately rinsed with de-ionized water to remove any residual salt from the surface, and dried in air at room temperature.

Results and Discussion

1-Optical Properties

1-1- AFM Images

Figure 1 shows the AFM images for the surface morphologies of ZnO nanowire arrays at different annealing temperatures of the thin films. It is notable that the ZnO nanowire arrays on the ZnO thin films annealed at 130 °C are well aligned vertically (Figure 1(a)), and the well defined crystallographic planes, providing a strong evidence that the nanowire arrays orientate along the c-axis. This implies its perfect *c*-axis orientation. As the annealing temperatures of the ZnO thin films increase from 130 to 900°C, the diameters of the ZnO nanowire arrays increase from 10 to 80 nm in average and its high ranging from 300 to 400 nm. The reason may be that the high annealing temperature evidently increase the interaction among the grains and leads the grains to merge together to form bigger ZnO seeds, and thus increases the diameter of the ZnO nanowires.

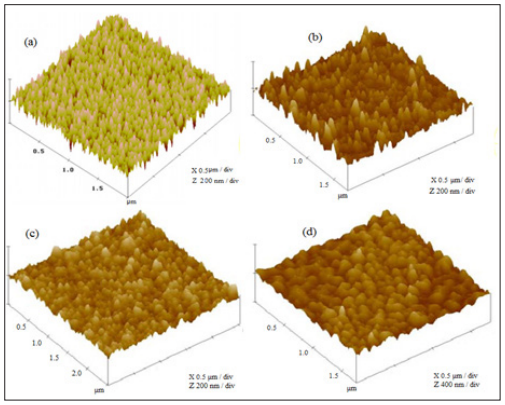

Figure1: AFM images of ZnO after growth Nanowires arrays(seed layer anneling at different temperature (a) t= 130 °C , (b) t= 300 °C, (c) t= 600 °C, (d) t= 900 °C)

1-2- PL Spectra

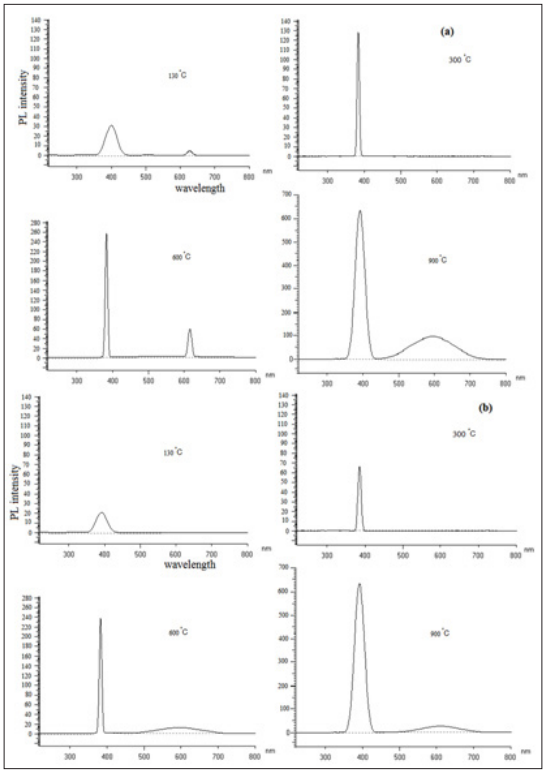

Figure 2: PL spectra of (a) ZnO seed layer and (b) ZnO nanowire arrays with annealing temperature of ZnO seed layers from 130 to 900 °C (excitation wavelength: 260 nm).

Figure 2(a) shows the PL spectra of ZnO thin films annealed at different temperatures. From this figure, an evident ultraviolet near-band edge emission peak at 382 nm is observed, which originates from the excitonic recombination. As the annealing temperature increasesfrom 130 to 900°C, the PL peak in the UV region is gradually getting higher. It is suppose that the higher annealing temperatures help the peregrination of grain boundaries and promote the aggregation of small crystals, and thus reduce the concentration of nonradiative recombination centers. However, at the temperature of 900°C, defects related to deep-level emission around 500–700 nm for the ZnO nanowire arrays were also observed. At the temperatures of 130 °C, the ZnO thin films may not form a good crystal phase, and hence the UV emission intensity is very low. Therefore, we may conclude that as the thin-film annealing temperature increases the UV emission peak increases but the peak in the green region also increases and its wide increases, that indicate the oxygen vacancies abruptly increase at high temperature. Figure (2) Shows that PL peak at wavelength (382 nm) is intense and narrow which mean the dimeter of nanowire are nearly homogenous and have approximately the same high. The PL characteristics of ZnO nanowire arrays with different annealing temperatures of thin films are shown in Figure 2(b). The UV emission peak increases with annealing temperature. The UV emission of ZnO nanowire arrays corresponding to the near-band edge emission is due to the recombination of free excitons through an exciton collision process. At the temperature of 900 °C, the defect-related green emission of the nanowire arrays is lower than that of the seed layers. The green emission is also known to be a deep level emission caused by the structural defects in the crystal such as oxygen vacancies, Therefore, it is suggested that the nanowire arrays may reduce the defect density and lower the defect-related emission caused by the thin films. At low temperatures of 130 and 300°C, the ZnO thin films exhibits a larger UV emission than ZnO nanowire arrays.

2- Electrical properties

2-1- (I-V) Curves for ZnO Nanowire arrays

I-Vcharacteristics of Nanowires ZnO arrays measured at room temperature are shown in Figers 3, 4 ,5 and 6.

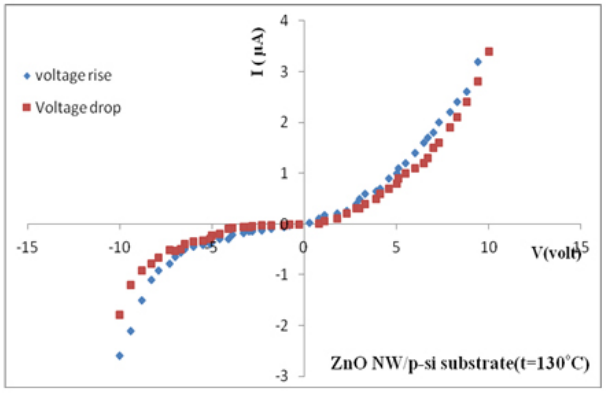

Figure 3: I-V characteristics of Nanowires ZnO that seed layer annealing at 130 ^{O}C

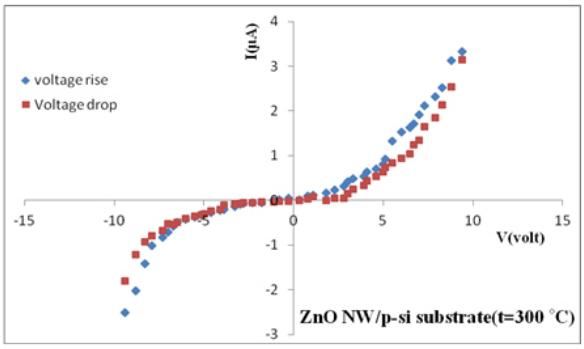

Figure 4: I-V characteristics of Nanowires ZnO that seed layer annealing at 300 ^{O}C

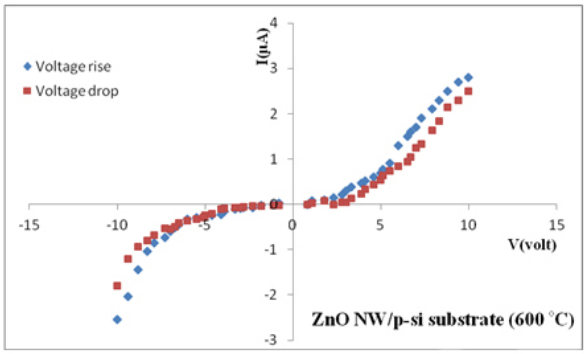

Figure 5: I-V characteristics of Nanowires ZnO that seed layer annealing at 600 ^{O}C

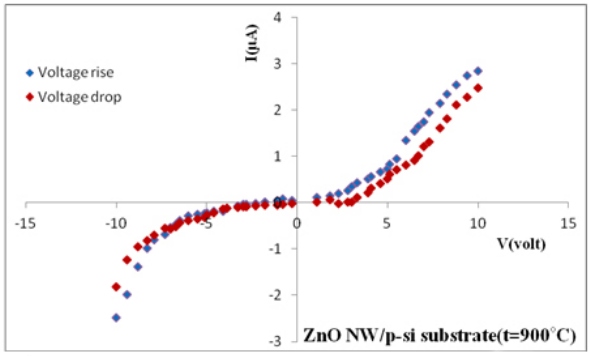

Figure 6: I-V characteristics of Nanowires ZnO that seed layer annealing at 900 ^{O}C

Figure (3,4,5,6) show that at constant voltage, the current value of the voltage is increase than its value in case of voltage decrease there is a slow loop. This is due to the fact that while lifting the applied voltage, the ions on the trap level have moved to another more closely related Crystalline structure leading to decreasing charge carriers during thedecrease in applied voltage and thus the current decline. Note from the (I-V) characteristic that the material behaves *p-n* junction diode .

As per the Sah–Noyce–Shockley theory,[11] the forwardcurrent in a p-n junction is dominated by recombination ofminority carriers injected into the neutral regions of the junction.This type of current gives an ideality factor of 1.0.Recombination of carriers in the space charge region, mediatedby recombination centers located near the intrinsicFermi level, results in an ideality factor of 2.0.

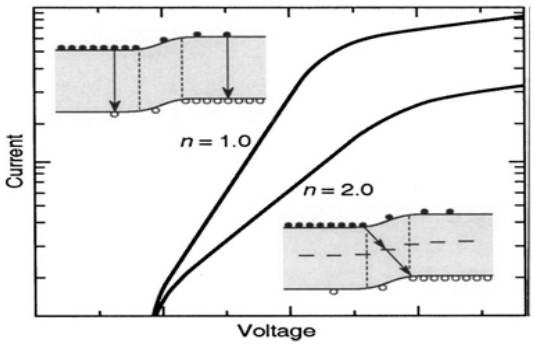

Figure 7: Schematic representation of *I-V* characteristics and carrier transport mechanism for diode ideality factors of *n*=1.0 and *n*=2.0.

The high ideality factors (n>>2.0) in LEDs or p-n junction diode were attributed to deep-level-assisted tunneling, due to temperature-independent slopes of (log *I*)-versus-*V* plots. Ideality factors close to 2.0 were attributed to space charge region recombination, consistent with the Sah–Noyce–Shockley theory, due to temperature-dependent slopes of (log *I*)-versus-*V* plots. However, a comprehensive theory for the high ideality factors found experimentally in *p-n* junctions has not been presented. the ideal factor can be calculated by drawing the graph of Ln(I) with V as in Figure (8)

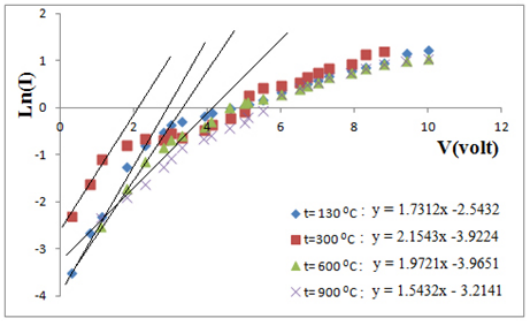

Figure 8: (Ln(I)-V) in the forward bias voltage range at voltage rise.
The ideal factor of the equation (1) can be calculated

$$Ln(I) = \frac{q/kT}{n} V \qquad (1)$$

Where q is the elementary charge, k is the Boltzmann constant, T is the absolute temperature, and n is the ideality factor.

Where attention is given to the linear area of the curve [12] . The ideal factor values were arranged in Table (1)

Table(1): Ideal factor values

Temperature	130 °C	300 °C	600 °C	900 °C
Ideal factor	22.81	18.33	20.02	20.02

it is apparent that ideality factors >> 2.0 can be measured, that was attributed to tunneling via deep levels in the forbidden gap.

2-2- Impedance spectra scope megerment

Using a GAIN PHASE ANALYZER devise type (Schlumberger-SI1253) with detection resistance R_d. A variable frequency signal [0.1 Hz -20KHz] was applied to the material and a fixed input voltage (V1 = 5v) was applied. To determine the spectrum of impedance spectra ,the equation (2) can be used

$$Z(\omega) = R(\omega) + jX(\omega) \qquad (2)$$

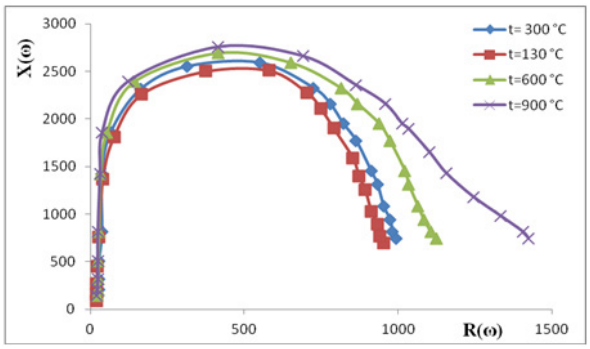

Figure 9: Impedance spectra scope of ZnO Nanowires arrays growth on p-Si

Figure 9. shows the spectrum of the Impedance resistance that the curve does not represent a regular semicircle and this indicates that the structure of the material is not regulated granules but rather is in a different form which is the nanowires [13].

The time of deceleration (τ) of the electron can be determined by drawing the real section of the impedance with frequency, since the deceleration time is equal to the inverted frequency at the top of the curve.

$$\tau = \frac{1}{f}$$

Table(2): Deceleration time values at different annealing temperature

t (°C)	130	300	600	900
R(ω)	2509.161	2589.161	2690.87	2755.87
f (Hz)	183.5	198.5	250.1	309.1
τ (sec)	0.005449	0.005037	0.003998	0.003235

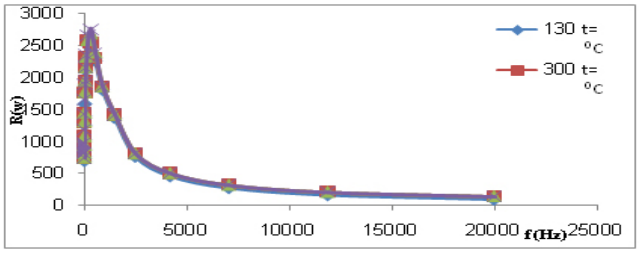

Figure 10: The real section of Impedance with Frequency of ZnO Nanowires arrays growth on p-Si

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